Direct Transfer Printing with Metal Oxide Layers for Fabricating Flexible Nanowire Devices

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A direct printing method for fabricating devices by using metal oxide transfer layers instead of conventional transfer media such as polydimethylsiloxane is presented. Metal oxides are not damaged by organic solvents; therefore, electrodes with gaps less than 2 μm can be defined on a metal oxide transfer layer through photolithography. In order to determine a suitable metal oxide for use as transfer layer, the surface energies of various metal oxides are measured, and Au layers deposited on these oxides are transferred onto polyvinylphenol (PVP). To verify the feasibility of our approach, Au source–drain electrodes on transfer layers and Si nanowires (NWs) addressed by the dielectrophoretic (DEP) alignment process are transferred onto rigid and flexible PVP-coated substrates. Based on transfer test and DEP process, Al_2O_3 is determined to be the best transfer layer. Finally, Si NWs field effect transistors (FETs) are fabricated on a rigid Si substrate and a flexible polyimide film. As the channel length decreases from 3.442 to 1.767 μm, the mobility of FET on the Si substrate increases from 127.61 ± 37.64 to 181.60 ± 23.73 $cm^2 V^{-1} s^{-1}$. Furthermore, the flexible Si NWs FETs fabricated through this process show enhanced electrical properties with an increasing number of bending cycles.

1. Introduction

Over the past few decades, a plethora of nanostructures including nanoparticles, nanowires (NWs), nanotubes, and nanosheets have been widely studied as building blocks for nanoelectronic devices such as field-effect transistors (FETs),[1–4] photosensors,[5] solar cells,[6–10] biosensors,[11–14] and light-emitting diodes[15–17] owing to their outstanding electrical and optical properties. In particular, nanomaterials are the most attractive for use in plastic electronics because of their mechanical flexibility and feasibility for printing on plastic substrates, enabling low-cost and large-area manufacturing, in contrast to the flat and rigid counterparts. It involves the development of transfer printing techniques and micro/nanofabrication of nanomaterials. To transfer nanomaterials to plastic substrates, polydimethylsiloxane (PDMS) is typically used as a stamp to deliver them in printed electronics applications because it is soft and elastic, facilitating precise transfer to the desired position through conformal contact.[18–20] At present, photolithography and PDMS-mediated transfer techniques are popularly used to fabricate devices based on nanomaterials. However, during the transfer processes, photolithography cannot be used on PDMS, because the photoresists, developers, and strippers are solutions containing organic solvents, which lead to the swelling of PDMS.[21] Therefore, defining patterns with features of submicron size or less on PDMS through photolithography remains challenging.

Here, to overcome the above flaw of PDMS, we suggest metal oxide transfer layers as candidates for replacing PDMS. Metal oxides, as well known, have a wide range of selection, and they can be prepared through various methods.[22–25] In this study, five different metal oxides (Al_2O_3, Nb_2O_5, ZnO, NiO_x, and WO_3) were investigated. Although there are many types of metal oxides, we used the most common materials; however, our approach can be applied for other oxides as well. Furthermore, through our approach, the phase of the metal oxide can be easily controlled, which helps modulate the morphology and surface energy. The most important variable for transfer media is the surface energy. Therefore, if a metal oxide layer could be applied, it can easily be optimized as the transfer layer. Metal oxides are not damaged by organic solvents, making it possible to achieve micro patterns with short gaps on transfer media through photolithography. Finally, FETs can be fabricated using this method for improved performance.

2. Results and Discussion

Figure 1a schematically describes the fabrication of an Si nanowire (NW) field-effect transistor (FET) array using a direct printing method with thin inorganic metal oxide layers. To verify the applicability of metal oxide layers to a transfer medium of gold electrodes, the surface characteristics were

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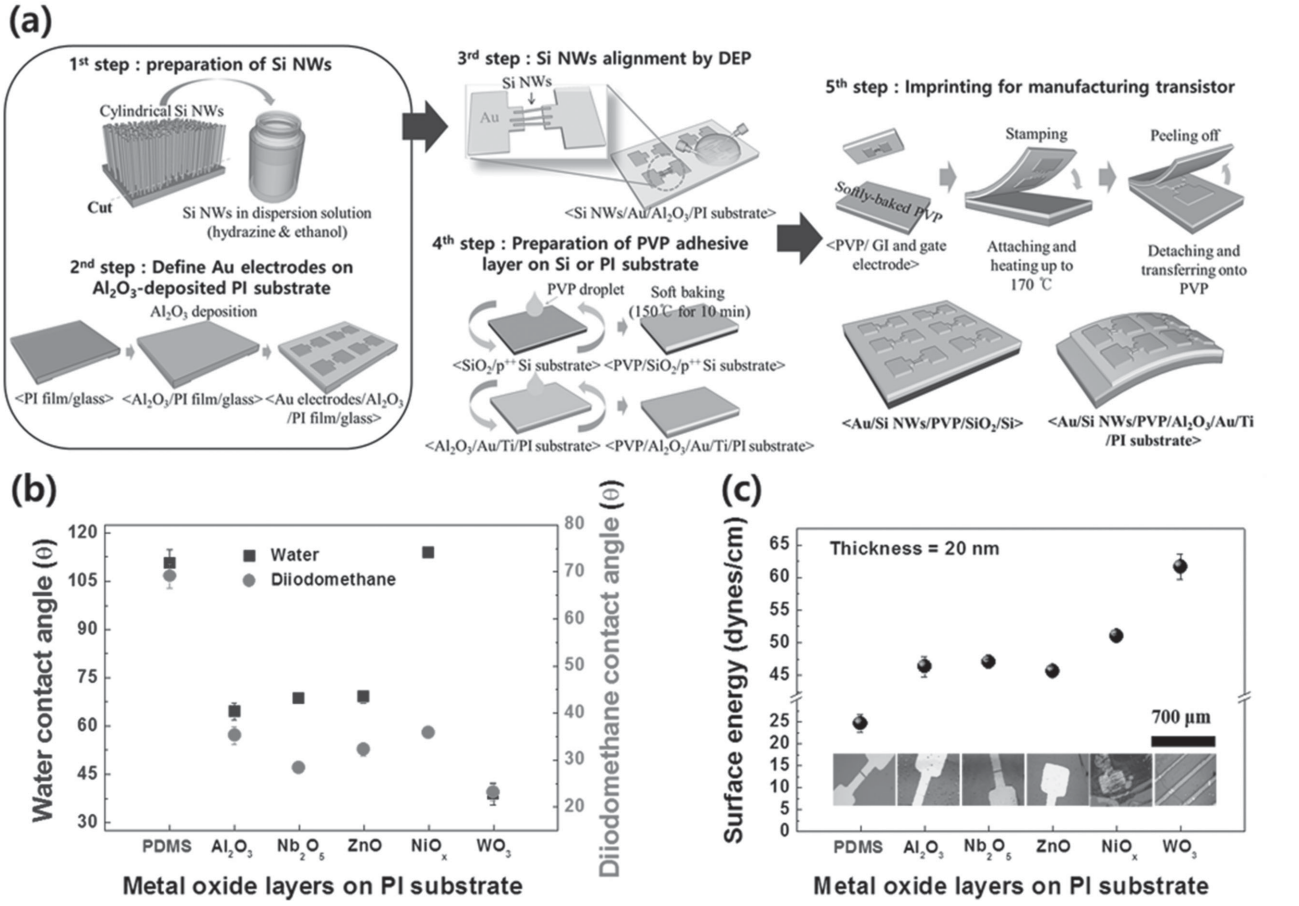

Figure 1. a) Process for the fabrication of Si NWs FET using a direct printing method. b) Contact angles of water and diiodomethane on metal oxide layers; Al_2O_3, Nb_2O_5, ZnO, NiO_x, and WO_3. c) Surface energies of each layer calculated by the Owen–Wendt model. The inset of (c) shows OM images of Au electrodes transferred to a PVP adhesive layer from each layer; PDMS, Al_2O_3, Nb_2O_5, ZnO, NiO_x, and WO_3, respectively.

investigated by comparing the surface energies of metal oxides and PDMS. Five different metal oxide layers (Al_2O_3, Nb_2O_5, ZnO, NiO_x, and WO_3) were deposited through RF magnetron sputtering. To evaluate the surface energy, the contact angles of water and diiodomethane were measured for the metal oxides and PDMS. The contact angle depends not only on the surface energy of the materials but also on the surface roughness. If the surface is rough, the liquid droplets for contact angle measurements spread over the surface, decreasing the contact angle. In this case, the surface energy becomes greater than the actual value. The rms roughness of PDMS was 0.48 nm, while that of the metal oxides was found to be 200–400 nm through atomic force microscopy (Figure S1, Supporting Information). This reveals that all metal oxides have a sufficiently smooth surface, minimizing the influence of surface roughness on the surface energy. The contact angles of water and diiodomethane were measured to be 110.71° ± 4.10° and 69.14° ± 2.52°, 64.41° ± 2.60° and 35.2° ± 1.92°, 68.48° ± 0.88° and 28.39° ± 0.81°, 69.03° ± 1.99° and 32.23° ± 1.35°, 113.83° ± 1.02° and 35.76° ± 0.72°, and 38.80° ± 3.19 and 23.2° ± 1.79° for PDMS, Al_2O_3, Nb_2O_5, ZnO, NiO_x, and WO_3, respectively (Figure 1b). Based on these values, the surface energies were calculated by using the following Owen–Wendt model (Figure 1c):[26]

$$\gamma_L(1+\cos\theta) = 2\sqrt{\gamma_S^d \gamma_L^d} + 2\sqrt{\gamma_S^p \gamma_L^p} \quad (1)$$

$$\gamma_S = \gamma_S^d + \gamma_S^p, \gamma_L = \gamma_L^d + \gamma_L^p, \quad (2)$$

where θ is the contact angle of the liquid droplet on the metal-oxide layer, γ_L is the surface energy of the liquid droplet, γ_S is the surface energy of the metal-oxide layer, γ_L^d and γ_L^p represent the dispersion and polar terms of the surface energy of the liquid, respectively, and γ_S^d and γ_S^p represent the dispersion and polar terms of the surface energy of the metal-oxide layer, respectively. The values of γ_L^d and γ_L^p are 22.85 and 50.3, and 48.5 and 2.3 dynes cm^{-1} for water and diiodomethane, respectively.[27] PDMS showed the lowest surface energy of 24.62 dynes cm^{-1}. The surface energies of Al_2O_3, Nb_2O_5, and ZnO were found to be 45.63 ± 0.72–47.00 ± 0.45 dynes cm^{-1}, whereas WO_3 had the highest surface energy of 61.68 dynes cm^{-1}. This implies that, among the metal oxides used in this study, Al_2O_3, Nb_2O_5, and ZnO could be used as transfer media. For Al_2O_3, Nb_2O_5, and ZnO, which have surface energies of 45.63 ± 0.72–47.00 ± 0.45 dynes cm^{-1}, the gold layers can be transferred on polyvinylphenol (PVP) receiver substrates (inset of Figure 1c), which are similar to that in case of the PDMS with low surface energy and thus show weak adhesion with

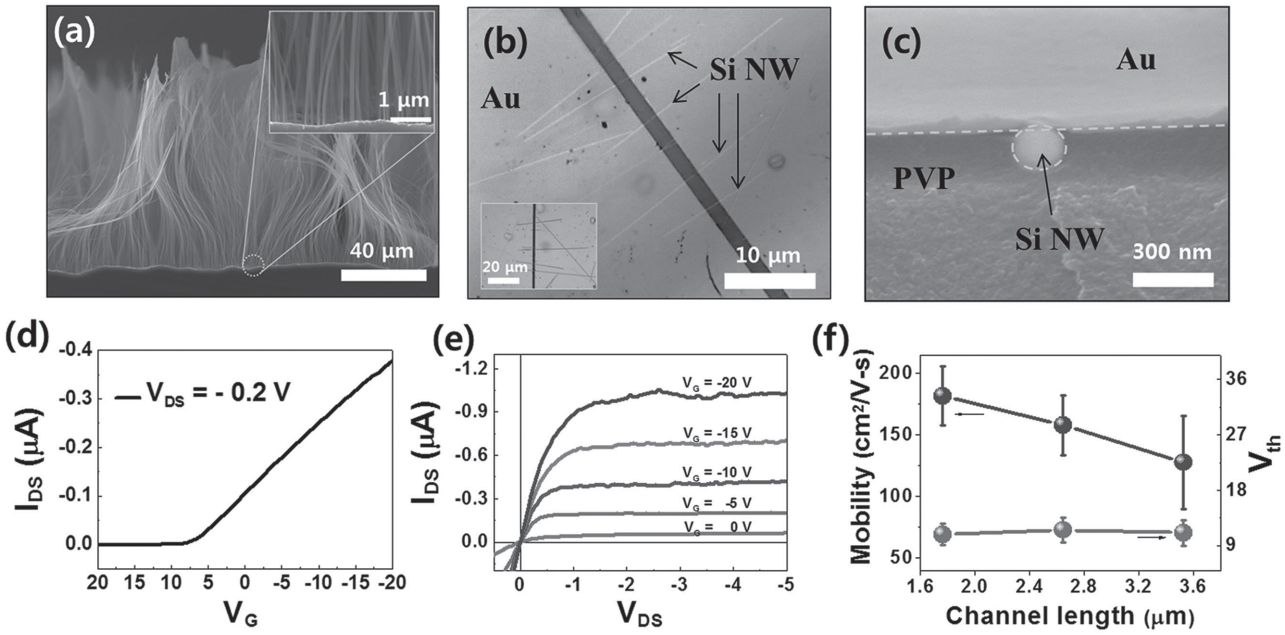

Figure 2. a) A cross-sectional SEM image of Si NWs etched for 2.5 h. Inset: High magnification SEM image of the yellow circled part. b) OM image of transferred Si NWs and Au electrodes onto a PVP adhesive layer. Inset: Aligned Si NWs on Au electrodes before transferring. c) A cross-sectional SEM image of a Au electrode and a Si NW partially embedded in PVP. d) Transfer and e) output characteristics of the Si NWs FET. f) Mobility and threshold voltage changes as a function of the channel length.

gold.[28] On the other hand, NiO_x and WO_3 films with surface energies above 50 dynes cm^{-1} cannot stamp the gold electrodes onto the PVP layer because of the strong adhesion between them (inset of Figure 1c).

Si NW FETs were fabricated on rigid Si and flexible polyimide (PI) substrates through a direct printing process with the metal-oxide stamps, where Al_2O_3, Nb_2O_5, and ZnO were tested as transfer media. First, the Si NWs were synthesized through a metal-assisted etching method from a boron-doped p-type Si wafer.[29] Their average diameter and length were observed to be 130 nm and 100 μm, respectively (**Figure 2**a; Figure S2a, Supporting Information). Because of their high aspect ratio of 780, the Si NWs were bent like hair (Figure 2a), indicating flexibility because of the nanoscale size, in contrast to rigid Si films. The Si NWs have rough surfaces and are single crystalline, growing along the ⟨100⟩ direction (Figure S2b,c, Supporting Information). The Si NWs were subsequently aligned on the Au electrodes, which were patterned on a metal oxide layer by using the standard photolithography technique through the dielectrophoretic (DEP) alignment process. Then, Si NWs and Au electrodes were transferred on a PVP-coated substrate with a gate electrode and gate insulating layer. Although ZnO and Nb_2O_5 could be appropriate transfer layers in terms of the surface energies mentioned above, they are not suitable for the DEP alignment process because of their semiconducting properties (Figure S3, Supporting Information). A strong electric field should be produced between the electrodes to align the Si NWs perpendicular to the Au electrodes by using the DEP process, for which insulating materials are required. Therefore, Al_2O_3, which has a large bandgap (8.8 eV) and a high dielectric constant (9.0–10.1), could be the best metal-oxide material for this process (inset of Figure 2b). The Si NWs aligned between Au electrodes on the surface of the Al_2O_3 layer were transferred onto a target substrate with the PVP layer by pressing the Al_2O_3 stamp with pressure. Since the adhesion between Au and Al_2O_3 was sufficiently weak, the Au electrodes were also stamped together with the Si NWs (Figure 2b), and the exposed area of the Si NWs were embedded in the PVP layer (Figure 2c).

This inorganic stamp enables the formation of source and drain electrodes with narrower gaps compared to the PDMS stamp because the inorganic stamp is not damaged by organic solvents, which are used in standard photolithography techniques. Within the resolution limits of our equipment, electrodes with gaps of 1.767, 2.604, and 3.442 μm were patterned on the Al_2O_3 layers, and by stamping, the Si NW FETs were fabricated with a back-gated configuration (Figure S4, Supporting Information). Figure 2d,e shows the transfer (I_{DS}–V_G) and output (I_{DS}–V_{DS}) curves of the FET, respectively, with a channel length of 1.767 μm. The value of I_{DS} increased with increasing negative V_G and saturated with increasing negative V_{DS}, indicating typical p-channel behavior and good ohmic contact between the Au electrodes and Si NWs. The on/off current ratio and field-effect mobility (μ_h) were calculated to be 1.2×10^7 and 176.94 $cm^2\ V^{-1}\ s^{-1}$, respectively.[30] As the channel length decreased from 3.442 to 1.767 μm, the mobility increased from 127.61 ± 37.64 $cm^2\ V^{-1}\ s^{-1}$ to 181.60 ± 23.73 $cm^2\ V^{-1}\ s^{-1}$ (Figure 2f). This enhanced mobility is due to the reduction of contact resistance in shorter-channel devices because the Si NWs used in this study have identical length, thereby increasing the contact area between the Au electrode and the Si NWs with decrease in the electrode gap.[31] Furthermore, as the Si NWs synthesized through a metal-assisted

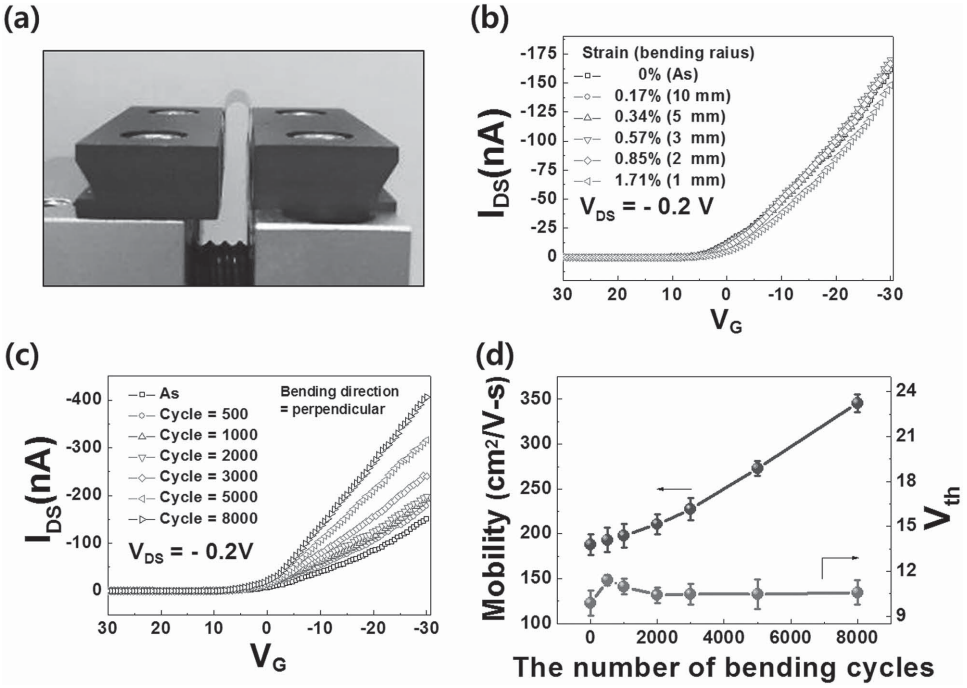

Figure 3. a) Photography of flexible Si NWs FET on a bending machine. Transfer characteristics of flexible Si NW FETs as a function of b) bending radius and c) the number of bending cycles in perpendicular direction with 0.57% strain. d) Mobility and threshold voltage changes with repeated bending cycles.

etching method have rough surfaces, the carriers would be trapped on the surface defects. Hence, a decrease in the channel length leads to the reduction of charge-trapping sites, resulting in increased mobility.[32] In addition, because the Si NWs have similar conduction properties including surface charges, the threshold voltage remains unchanged regardless of the channel length.[33]

In order to demonstrate the feasibility of this process for flexible electronics, Si NW FETs were fabricated on a PI substrate through direct printing with an Al_2O_3 layer as the transfer medium, as shown in **Figure 3**a. Figure 3b,c shows the transfer curves of the Si NW FETs as functions of bending strain (bending radius) and cycle, respectively. The transfer curves did not show a large current variation over the range of bending strain up to 0.85%, from which the mobilities were estimated to be 192.46 ± 7.74 $cm^2\ V^{-1}\ s^{-1}$. When the bending strain exceeded 1.71%, the transfer curve became degraded, and the mobility decreased to 176.32 $cm^2\ V^{-1}\ s^{-1}$. In addition, the value of I_{DS} in the transfer curves and the resulting mobilities gradually increased with the bending cycles up to 8000 at 0.57% strain. After 10 000 bending cycles, the device irreversibly failed.

Typical flexible devices show the degradation in electrical properties as the bending cycles are increased, while flexible Si NW FETs fabricated through the proposed process exhibit enhanced electrical properties with increasing bending cycles. After 8000 cycles of a bending test with 0.57% strain, the transfer current was increased by 266% at −30 V gate voltage compared to the current before bending, as shown in Figure 3c. The Si NWs linked on Au electrodes through the DEP process were in physical contact with the Au electrodes by the van der Waals force. The contact property was improved by the friction between the surface of the Si NWs and Au electrodes during bending, which resulted in the increase in mobility. Figure S5a (Supporting Information) shows that the current increases with increase in the bending cycle. The nonlinear *I–V* curve originated from the electron transport properties of the porous Si NWs.[34] Another possible reason of the improvement in the transfer current could be the increase in the capacitance of the gate insulator with the number of bending cycles, as shown Figure S5b (Supporting Information). After 8000 cycles of a bending test, the capacitance of the metal-insulator-metal (MIM) structure, as indicated in the inset of Figure S5b (Supporting Information), increased by 12.58%. The PVP polymer chain became aligned with repetitive bending, causing the increase in capacitance. With the compensated value of capacitance, the transistor mobility was 188.09 ± 11.59 $cm^2\ V^{-1}\ s^{-1}$ before the bending test; this value gradually increased to 345.54 ± 10.16 $cm^2\ V^{-1}\ s^{-1}$ after 8000 cycles of a bending test, as indicated in Figure 3d. However, we believe that the stress caused by bending was focused on the interface between Si NWs and PVP and that the capacitance in the device was enhanced further compared to that of the MIM structure because the actual structure of the flexible device is that of Si NWs embedded in PVP. In order to verify this hypothesis, the flexible device was bent in the parallel direction. Consequently, the transfer current was observed to be increased by 195% with increasing bending cycles, as shown in Figure S5c (Supporting Information). This result implies that the change in capacitance is dependent on the aligning direction of the embedded Si NWs as well as the bending direction.

3. Conclusion

In summary, we have investigated the surface energies of metal oxide layers used as the transfer layer for Au electrodes, and a transfer test was conducted to determine the most appropriate metal oxide layer. Al_2O_3, Nb_2O_5, and ZnO with surface energies of less than 50 dynes cm^{-1} were determined to be suitable materials. In particular, Al_2O_3, which has a high dielectric constant that helps form a strong electric field between Au electrodes, was chosen among Al_2O_3, Nb_2O_5, and ZnO as the transfer layer because the DEP alignment process was applied to address Si NWs. To verify the feasibility of our approach, FETs consisting of Si NWs were fabricated on both a PVP-coated Si substrate and a flexible PI film through the direct printing method with an Al_2O_3 transfer layer. On the rigid Si substrate, the mobility of FET linearly increased from 127.61 ± 37.64 cm^2 V^{-1} s^{-1} to 181.60 ± 23.73 cm^2 V^{-1} s^{-1} with decrease in the channel length from 3.442 to 1.767 μm because the carriers trapped on the rough surface of Si NWs were reduced and the contact area between Si NWs and Au electrodes was increased. In the case of the flexible Si NW FET, the electrical properties were maintained over the bending-strain range up to 0.85%, and the degradation in current started with bending strains greater than 1.71%. Furthermore, after 8000 cycles of a bending test with 0.57% strain in the perpendicular direction, the transfer current of the flexible FET increased by 266% at −30 V of gate voltage. The reason for this phenomenon is the improved contact property between the Si NWs and Au electrodes as well as the increased capacitance of the gate insulator during the bending test.

4. Experimental Section

Preparation of Metal Oxide Layers on Flexible PI Substrates: As transfer media for direct printing, five different metal oxides (Al_2O_3, Nb_2O_5, ZnO, NiO_x, and WO_3) were used. A 15 μm thick flexible PI substrate was cleaned by sonication in acetone, methanol, and deionized water for 10 min each, and was then blown to dry with nitrogen gas. All the metal oxide films were deposited on the PI substrates by radio frequency (RF) magnetron sputtering at an RF power of 150 W at a working pressure of 10 mTorr. The thickness of all the deposited films was about 20 nm in order to obtain high flexibility and smooth surface. For comparison, 5 mm thick PMDS was prepared as a conventional transfer medium by mixing SYLGARD 184 silicon elastomer curing agent and SYLGARD silicon elastomer base with a volume ratio of 1:10 and baked at 75 °C for 1 h. The contact angles of water and diiomethane on PDMS, Al_2O_3, Nb_2O_5, ZnO, NiO_x, and WO_3 were measured by using a contact angle analyzer (phoenix 300 plus SEO Co., Ltd.). And the surface roughnesses of metal oxide layers were measured by using atomic force microscopy (MFP-3D, Asylum research).

Direct Transfer Printing of Au Electrode Patterns Using Metal Oxide Films: Au electrode patterns with gaps of 1.767, 2.604, and 3.442 μm were defined on the metal oxide films (Al_2O_3, Nb_2O_5, ZnO, NiO_x, and WO_3) and PDMS by photolithography followed by electron-beam evaporation. As a receiver substrate, a PVP-coated substrate was prepared by two-step spin-coating 10% PVP solution with a cross-linking agent, poly(melamine-*co*-formaldehyde) in propylene glycolmonomethyl ether acetate on an Si substrate at 500 rpm for 5 s and then at 1500 rpm for 10 s, and it was softly baked at 150 °C for 10 min. The transfer media with the Au electrode patterns were contacted with the PVP-coated substrate under a pressure of 26.7 g cm^{-2}, and then heated at 170 °C with the increasing rate of 3.34 °C min^{-1}. Finally, the transfer media were peeled off, leaving the Au electrode patterns on the PVP-coated substrate.

Fabrication of Si NW FETs on Rigid or Flexible Substrates by Direct Transfer Printing Method: DEP process was used to align Si NWs between Au electrodes on an Al_2O_3 transfer medium. Si NWs were prepared by a metal-assisted etching method from a boron-doped p-type Si (100) wafer with a resistivity of 1–10 Ω cm as described previously.[29] The synthesized Si NWs were dispersed in the solution consisting of dilute hydrazine (0.05%) and ethanol, yielding 7×10^8 NWs mL^{-1}. After a 4 μL droplet was suspended on the Au electrode gaps, direct current (DC) bias (amplitude of 10 V_{pp}, frequency of 1 kHz, and pulse width of 500 μs) was applied for 5 s so that several Si NWs were aligned between Au electrodes. To fabricate Si NW FETs, a heavily p-doped Si substrate with a thermally grown 300 nm thick SiO_2 layer and a 15 μm thick PI substrate were used. For the PI substrate, a Ti/Au gate electrode was deposited on the PI substrate by an e-beam evaporator and an Al_2O_3 layer was deposited on gate electrodes as a gate dielectric. For direct transfer printing, PVP layer was coated onto the substrate by two-step spin coating at the same condition with a receive substrate. The aligned Si NWs and Au electrodes on the surface of the Al_2O_3 layer were subsequently attached onto the PVP-coated substrate by pressing the Al_2O_3 stamp with a pressure of 26.7 g cm^{-2} and then heated to 170 °C with the increasing rate of 3.34 °C min^{-1}. After peeling off transfer medium, finally, the devices were baked at 175 °C for 1 h. The morphology of the Si NWs and the structure of Si NWs imbedded in PVP were observed by using field-emission scanning microscopy (JSM-7001, Jeol). And *I–V* characteristics were measured by using a probe station (Desert Cryogenics, model TTP4) and an Agilent semiconductor parameter analyzer (B1500A).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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